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April 13, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: Stephen B. Ackerman, Reg. No. 37,761
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No.	09/912,737	07/26/2001
L. GOH ET AL		
"A METHOD TO IMPROVE ADHESION OF DIELECTRIC FILMS IN DAMASCENE INTERCONNECTS"		
Grp. Art Unit: 2822	J. L. BROPHY	

OK to enter /JLB 5/24/04

RESPONSE FINAL PATENT OFFICE ACTION

Dear Sir:

In response to the Office Action dated February 13, 2004, please amend the above-identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 13, 2004.

Rosemary L. S. Pike. Reg # 39,332

Signature Rosemary L S Pike

Date April 13, 2004

Amendments to the Claims are reflected in the listing of the Claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.

Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) A method of forming a dielectric material layer comprising:

depositing a low dielectric constant material layer on a passivation layer on a substrate wherein said low dielectric constant material is selected from the group consisting of: porous or non-porous carbon-based silicon oxides, , porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said low dielectric constant material; and

thereafter depositing a TEOS-based silicon oxide layer overlying said low dielectric constant material whereby there is good adhesion between said low dielectric constant material layer and said TEOS-based silicon oxide layer.

2. (canceled)

3. (original) The method according to Claim 1 wherein said low dielectric constant material layer has a thickness of between about 500 and 50,000 Angstroms.

4. (original) The method according to Claim 1 wherein said step of implanting silicon ions into said low dielectric constant material layer comprises implanting said silicon ions

at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

5. (canceled)

6. (previously presented) The method according to Claim 1 wherein said TEOS-based silicon oxide layer has a thickness of between about 50 and 5000 Angstroms.

7-11. (canceled)

12. (currently amended) A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material layer over a substrate wherein said first low dielectric constant material is selected from the group consisting of: ~~porous or non-porous carbon-based silicon oxides,~~alkyl silsesquioxanes , porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said first low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide etch stop layer overlying said first low dielectric constant material whereby there is good adhesion between said first low dielectric constant material layer and said TEOS-based silicon oxide etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer wherein said second low dielectric constant material is selected from the group

consisting of: ~~porous or non-porous carbon-based silicon oxides,~~ alkyl silsesquioxanes, porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said second low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide capping layer overlying said second low dielectric constant material whereby there is good adhesion between said second low dielectric constant material layer and said TEOS-based silicon oxide capping layer;

forming a dual damascene opening through said capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

13. (canceled)

14. (original) The method according to Claim 12 wherein said first and second low dielectric constant material layers have a thickness of between about 500 and 50,000 Angstroms.

15. (original) The method according to Claim 12 wherein said steps of implanting silicon ions into said first and second low dielectric constant material layers comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

16. (previously presented) The method according to Claim 12 wherein said silicon ions are implanted into said first and second low dielectric constant material layers to a depth of between about 50 and 600 Angstroms thereby forming a roughened silicon-implanted surface of said first and second low dielectric constant material layers.

17. (previously presented) The method according to Claim 12 wherein said TEOS-based silicon oxide etch stop layer has a thickness of between about 50 and 5000 Angstroms.

18-22. (canceled)

23. (previously presented) The method according to Claim 12 wherein said TEOS-based silicon oxide capping layer has a thickness of between about 50 and 5000 Angstroms.

24. (currently amended) A method of forming a dielectric material layer comprising:

depositing a low dielectric constant material layer on a substrate wherein said low dielectric constant material is selected from the group consisting of: ~~porous or non-porous carbon-based silicon oxides,~~alkyl silsesquioxanes , porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said low dielectric constant material layer to a depth of between about 50 and 600 Angstroms thereby forming a roughened silicon-implanted surface of said low dielectric constant material layer; and

thereafter depositing a TEOS-based silicon oxide layer overlying said roughened surface of said low dielectric constant material whereby there is good adhesion between said low dielectric constant material layer and said TEOS-based silicon oxide layer.

25. (previously presented) The method according to Claim 24 wherein said low dielectric constant material layer has a thickness of between about 500 and 50,000 Angstroms.

26. (previously presented) The method according to Claim 24 wherein said step of implanting silicon ions into said low dielectric constant material layer comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

27. (previously presented) The method according to Claim 24 wherein said TEOS-based silicon oxide layer has a thickness of between about 50 and 5000 Angstroms.

28. (currently amended) A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material layer over a substrate wherein said first low dielectric constant material is selected from the group consisting of: ~~porous or non-porous carbon-based silicon oxides,~~ alkyl silsesquioxanes, porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said first low dielectric constant material layer to a depth of between about 50 and 600 Angstroms;

thereafter depositing a TEOS-based silicon oxide etch stop layer overlying said first low dielectric constant material whereby there is good adhesion between said first low dielectric constant material layer and said TEOS-based silicon oxide etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer wherein said second low dielectric constant material is selected from: ~~porous or non-porous carbon-based silicon oxides,~~alkyl silsesquioxanes , porous or non-porous organic polymers, and porous or non-porous inorganic polymers;

implanting silicon ions into said second low dielectric constant material layer to a depth of between about 50 and 600 Angstroms;

thereafter depositing a TEOS-based silicon oxide capping layer overlying said second low dielectric constant material whereby there is good adhesion between said second low dielectric constant material layer and said TEOS-based silicon oxide capping layer;

forming a dual damascene opening through said capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

29. (previously presented) The method according to Claim 28 wherein said first and second low dielectric constant material layers have a thickness of between about 500 and 50,000 Angstroms.

30. (previously presented) The method according to Claim 28 wherein said steps of implanting silicon ions into said first and second low dielectric constant material layers comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

31. (previously presented) The method according to Claim 28 wherein said TEOS-based silicon oxide etch stop layer has a thickness of between about 50 and 5000 Angstroms.

32. (previously presented) The method according to Claim 28 wherein said TEOS-based silicon oxide capping layer has a thickness of between about 50 and 5000 Angstroms.